SLIC Dial Pulse Performance

Advanced Micro Devices

Application Note

In an AMD SLIC-based line circuit, the opening and closing of the dial switch produces a stream of dial pulses at the ($\overline{DET}$) loop detector logic output pin. Before it begins decoding the dial pulses, the exchange processor must often eliminate false pulses caused by contact bounce in the dial switch.

To accomplish contact debouncing, the processor usually takes several samples during the period of each of the pulses emanating from the $\overline{DET}$ pin of the SLIC device. If the level at $\overline{DET}$ does not change for a given number of samples, then the $\overline{DET}$ level is interpreted as valid. It is necessary that the processor receives an adequate number of samples to accomplish this task. The amount of available time for processor debouncing is reduced when the SLIC device introduces a small amount of delay difference between loop-open and loop-closure detection. This delay difference results in what is commonly referred to as dial pulse distortion.

The purpose of this application note is to describe and quantify expected dial pulse distortion in an AMD SLIC-based line circuit. Using the data presented here, the linecard designer can optimize hardware and software for the best possible dial pulse performance.

PRIMARY FACTORS AFFECTING DIAL PULSE DISTORTION

Figure 1 is a simplified functional diagram showing the essential parts of the SLIC that determine dial pulse performance. For simplification, the diagram is only a single-ended representation of the longitudinally balanced, double-ended, two-wire circuit actually implemented.

This is a simplified single-ended model where only single pins A/B and HPA/B represent A, B, HPA, and HPB, respectively. The single current amplifier K1 represents the combination of the Line A and Line B power amplifiers that are actually on the chip.

If the dial switch shown in Figure 1 is in the closed position, current I_L flows through load resistor R_L. The DC-feed characteristics programmed by R_{DC1} and R_{DC2} determine the magnitude of this current that the line current sense amplifier detects as the voltage drop across resistor R_{SENSE}. The current sense amplifier feeds a current out of the R_D pin that is 292* times smaller than the actual loop current. Voltage V_{RD}, which is proportional to the loop current, is generated across resistor R_D. This voltage is compared, internally, to a 1.25-V reference. If V_{RD} is greater than the reference, the $\overline{DET}$ pin drops to a logic Low, indicating a switch closure. Capacitor C_D is connected across R_D to filter out any high-frequency noise components that may cause a false switch-closure or switch-open detection.

***Note:** Refer to the specific data sheet for each SLIC device for the actual value. 292 is standard for most SLIC devices.

Major dial pulse delays are introduced at the SLIC R_D pin as a result of the presence of capacitor C_D. Exponential rise and fall times of voltage V_{RD} cause delays between the time of a dial switch operation and the time when the $\overline{DET}$ output voltage reacts. As illustrated in Figure 2, the amount of time between a dial switch open and a logic High transition on the $\overline{DET}$ pin is Tdopen and the time from a dial switch on to a $\overline{DET}$ logic Low is Tdclosed. The difference between them (Tdopen – Tdclosed) is defined as the amount of dial pulse delay distortion in the system.

In addition to the dependence of the dial pulse delays on R_D and C_D, the delays also depend, to a large extent, on the level of DC current in the telephone line. A lower programmed loop current means less delay from a dial switch open to a logic High at the $\overline{DET}$ pin. The reason for this can be seen by observing the V_{RD} waveform in Figure 2. When the dial switch goes off, a lower level of loop current means a lower initial V_{RD} voltage that requires less time to decay to the 1.25-V reference level. Conversely, when the dial switch closes, a lower level of loop current means that V_{RD} is charging to a lower level and needs more time to reach the reference level.

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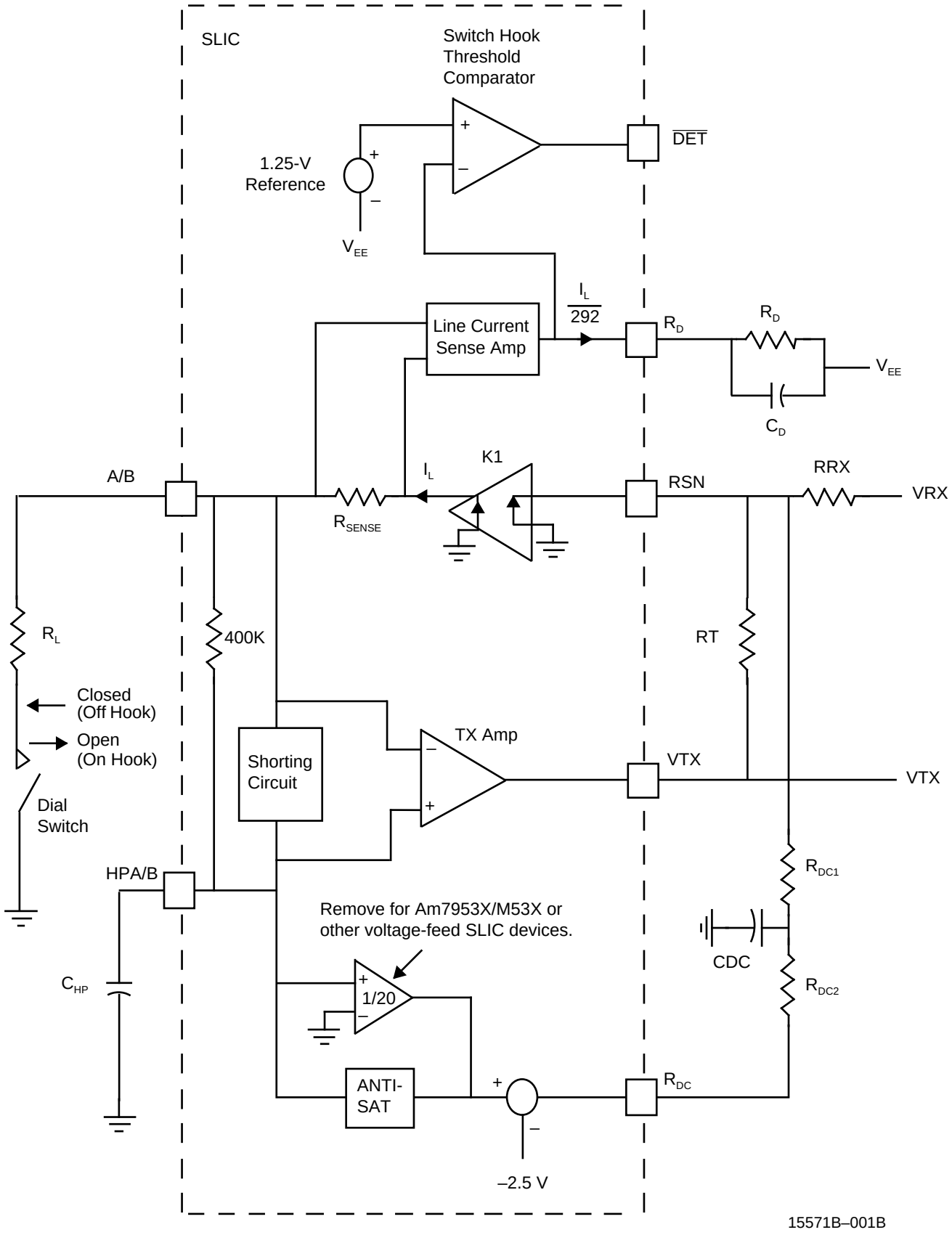

Figure 1. Simplified Functional Diagram for SLIC Dial Pulse Performance

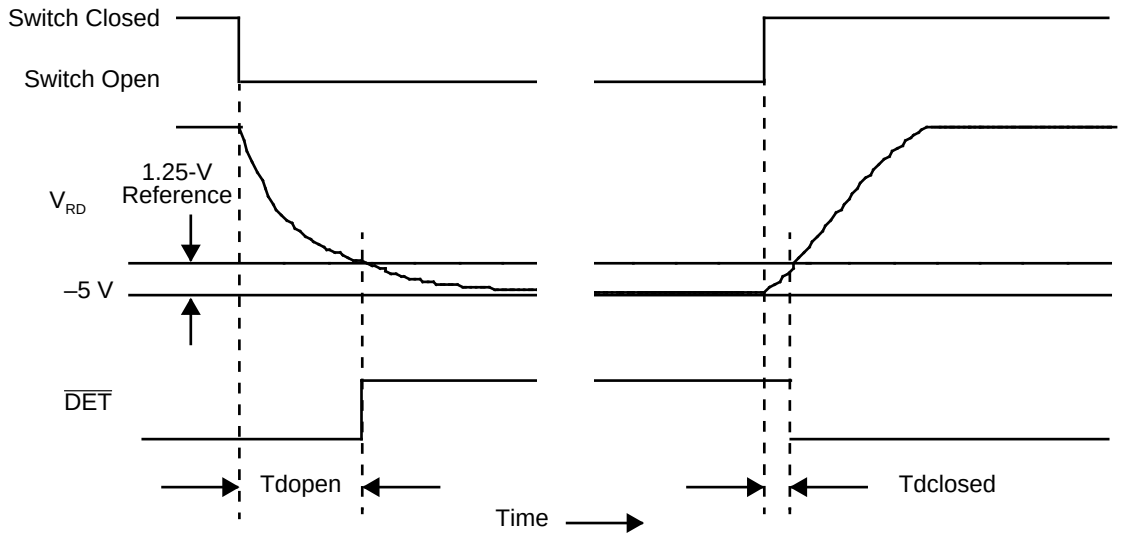

Figure 2. SLIC Dial Pulse Waveforms

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Equations 1a, 1b, and 2 describe the primary effects of R_D, C_D, and I_L on dial switch delay times and can be used to compute the values of Tdopen and Tdclosed shown in Figure 2.

$$Tdopen = R_D\ C_D = \ln\left(\frac{I_L\ R_D}{365}\right);\ I_L < \frac{1900}{R_D} \qquad (1a$$

$$Tdopen = 1.65\ R_D\ C_D;\ I_L \geq \frac{1900}{R_D} \qquad (1b$$

$$Tdclosed = R_D\ C_D\ \ln\left(1 - \frac{365}{I_L\ R_D}\right) \qquad (2$$

Because the voltage swing of V_{RD} is limited to approximately 6.5 V above V_{EE}, Equations 1a and 1b describe Tdopen. Equation 1a is valid below 6.5 V and Equation 1b is valid above 6.5 V.

Of course, these equations are valid only when I_L is greater than the loop detection threshold current determined by resistor R_D.

$$I_L > \frac{365}{R_D}$$

Secondary Factors

Equations 1a, 1b, and 2 only describe the primary causes of the dial pulse delay due to R_D, C_D, and loop current. However, components C_{HP}, R_{DC1}, R_{DC2}, C_{DC}, and the SLIC chip itself can create second order effects. These effects, under some line conditions, can be significant.

One factor is the shorting circuit in the SLIC device that activates when the voltage between the A and B pins suddenly changes because of a switch hook or a dial switch operation. This circuit helps the SLIC to quickly adapt to new levels of line current and line voltage. The currents flowing through this circuit can influence the dial pulse delay particularly at lower loop current detection threshold settings.

Immediately after a dial switch opening, current from the output amplifiers has no other course but to flow through the R_{SENSE} and shorting circuit while charging capacitor C_{HP}. This charge delays the detection of a dial switch opening.

After a switch closure, C_{HP} rapidly dumps its small charge through the trigger circuit into the load (not through R_{SENSE}). Therefore, C_{HP} does not introduce delay in the detection of a dial switch closure. Delay in this case results from the charging time of C_{DC}.

Figure 3 illustrates these effects by showing the response of V_{RD} with and without capacitor C_D connected. The V_{RD} waveform produced with C_D disconnected is an unfiltered representation of the actual current being delivered by the SLIC power amplifiers.

In Figure 3, the dial switch goes from closed to open at t = 0. Inspection of the C_D = 0 curve shows that the C_{HP} charging current begins at t = 0 and lasts for approximately 1.2 ms. V_{RD} will take longer to decay to the 1.25-V threshold level when C_D is connected. This causes Tdopen to increase slightly.

When the loop goes from switch open to switch closed, the output amplifiers try to deliver the programmed current. The amplifiers cannot do this immediately because of the charging of C_{DC} with a time constant τ_{dc} deter-

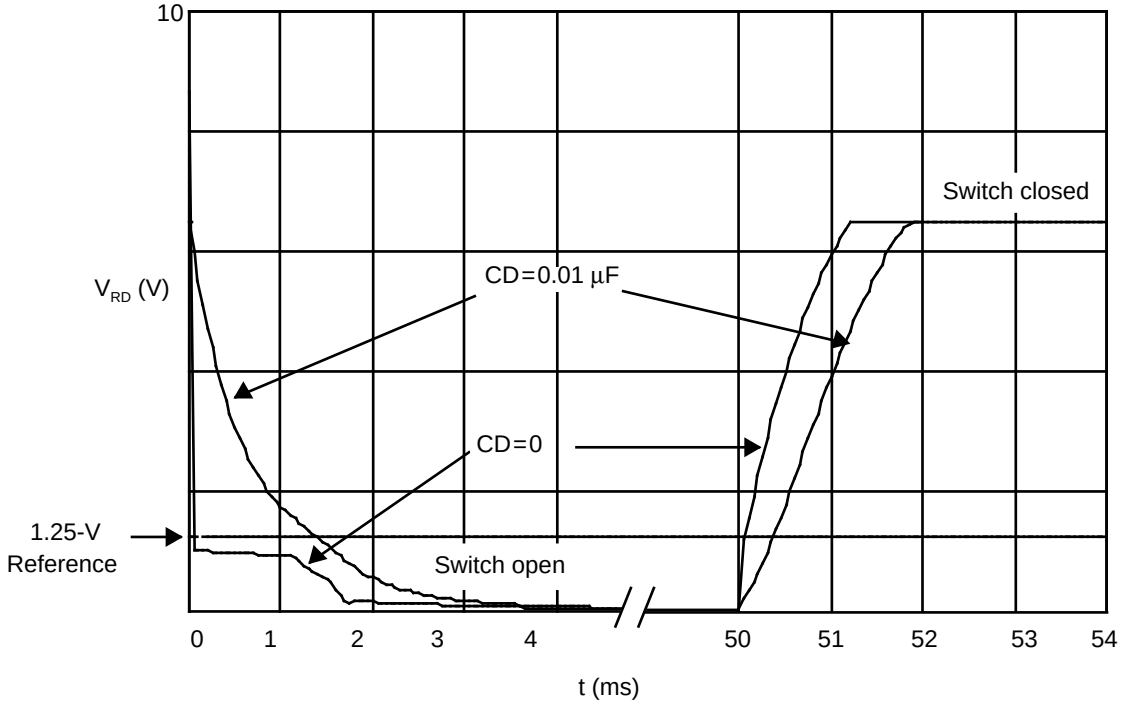

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Figure 3. Typical Response at SLIC R_D Pin (R_D=51.1 kΩ)

mined by R_{DC1}, R_{DC2}, and C_{DC}. The loop current rises with the same time constant to its final value. In this case, when

C_D is connected, Tdclosed will depend mainly on the delay caused by R_D and C_D, and on the delay caused by τ_{dc}.

The graphs of Figure 4a through Figure 4h show the typical dependence of dial pulse delays, Tdclosed and Tdopen, on loop current. Curves for two sets of R_D and C_D values are included for resistance feed and for current feed devices. The curves shown are valid only for Am7957X/Am79M57X resistance-feed SLIC devices and for Am7953X/Am79M53X current-feed SLIC devices intended for –48-V battery operation. These curves can be used to estimate dial pulse distortion for most circuit configurations and line conditions. (These curves may also apply to other AMD SLIC devices with similar gains and scaling constants. Consult individual data sheets for these parameters.)

As a reference, the ideal delay caused by R_D and C_D (described by Equation 2) is shown on each graph.

For example, assume the following conditions:

Loop current, $I_L = 40\ mA$

$R_{DC1} = R_{DC2} = 20\ k\Omega$

$C_{DC} = 0.15\ \mu F$

$C_{HP} = 0.33\ \mu F$

$R_D = 51.1\ k\Omega$

$C_D = 0.01\ \mu F$

$$\tau_{dc} = \frac{R_{DC1}\ R_{DC2}}{R_{DC1} + R_{DC2}}\ C_{DC} = 1000 \bullet 0.15 \bullet 10^{-6}$$

$$= 1.5 \bullet 10^{-3} = 1.5\ ms$$

Tdclosed (from Figure 4a) $= 0.75\ ms$

Tdopen (from Figure 4b) $= 1.35\ ms$

Dial pulse distortion = Tdopen – Tdclosed
$= 1.35\ ms - 0.75\ ms = 0.6\ ms$

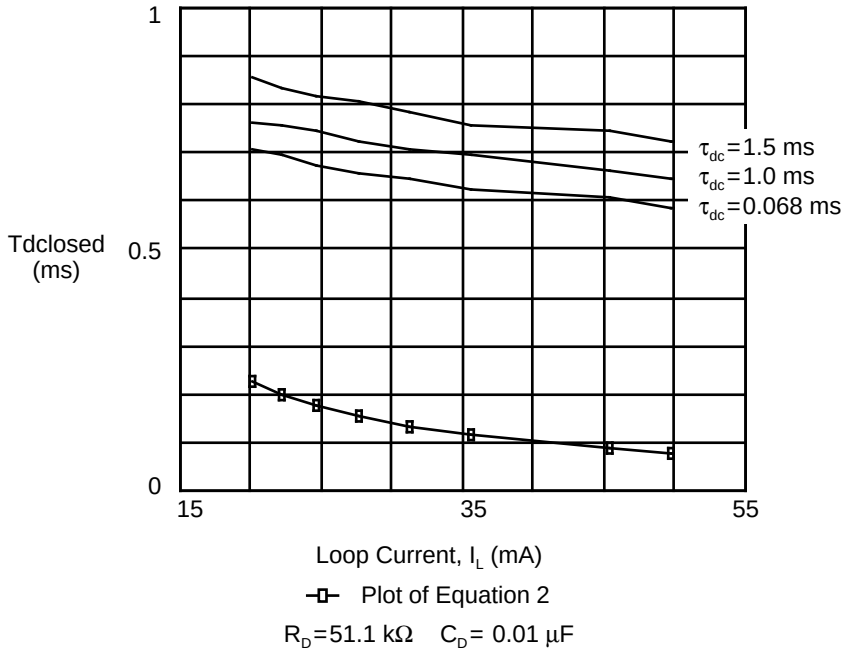

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Figure 4a. Tdclosed versus I_L for Various τ_{dc} (Resistance Feed Devices)

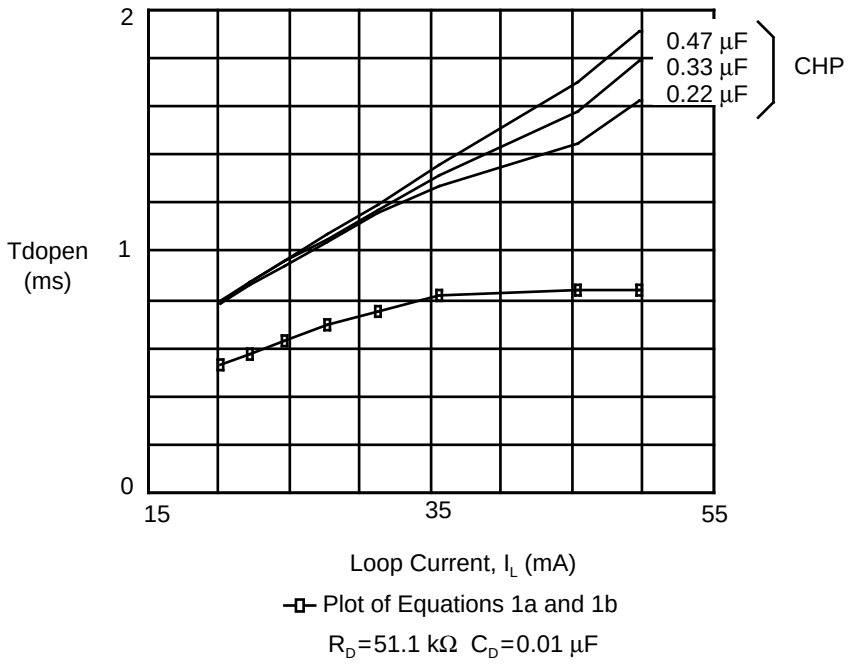

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Figure 4b. Tdopen versus I_L for Various C_{HP} (Resistance Feed Devices)

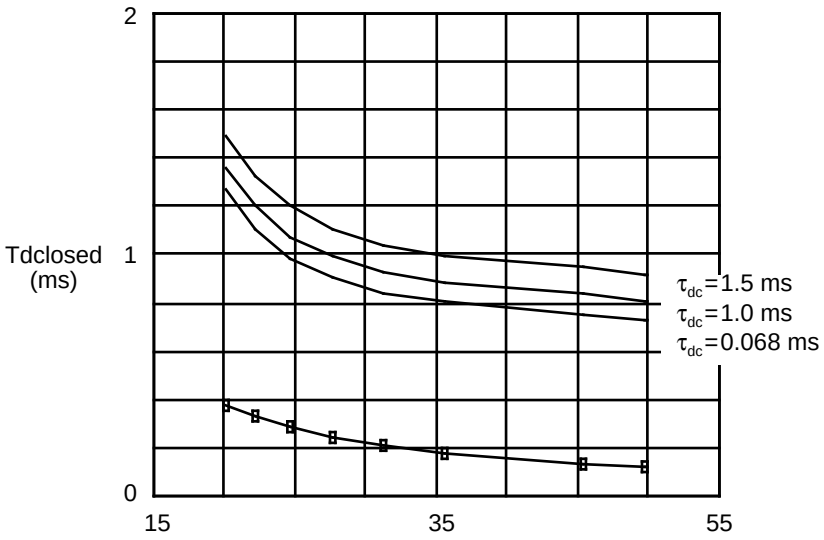

Figure 4c. Tdclosed versus I_L for Various τ_{dc} (Resistance Feed Devices)

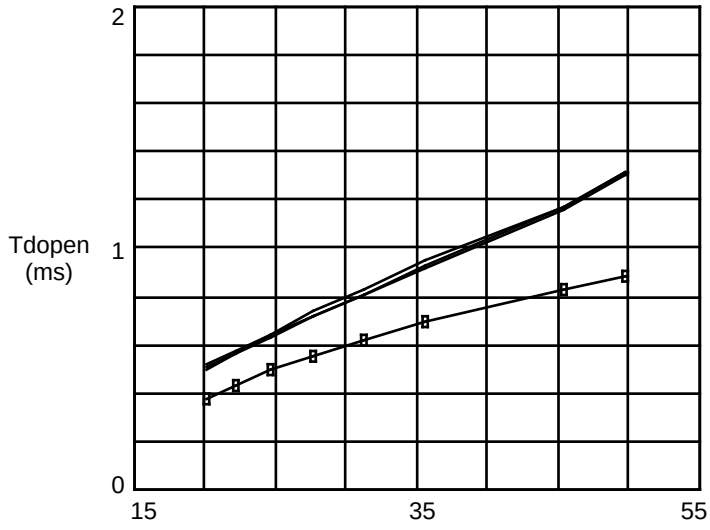

Figure 4d. Tdopen versus I_L (Resistance Feed Devices)

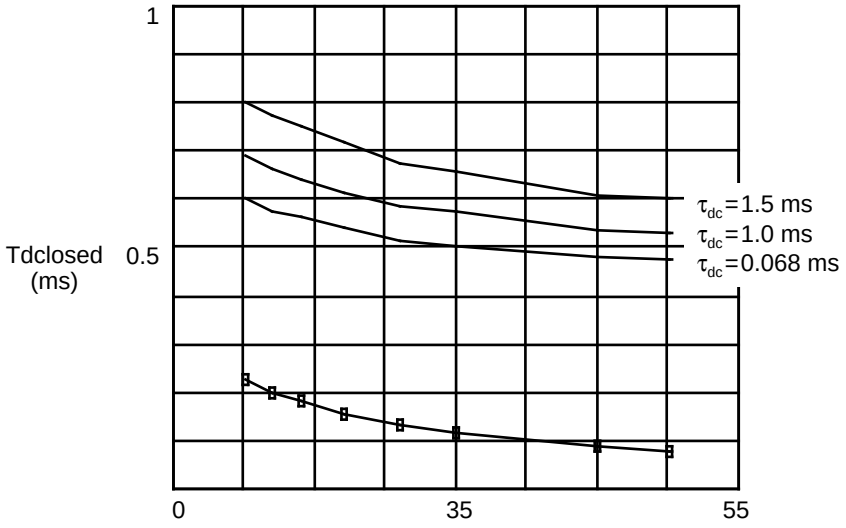

Figure 4e. Tdclosed versus I_L for Various τ_{dc} (Current Feed Devices)

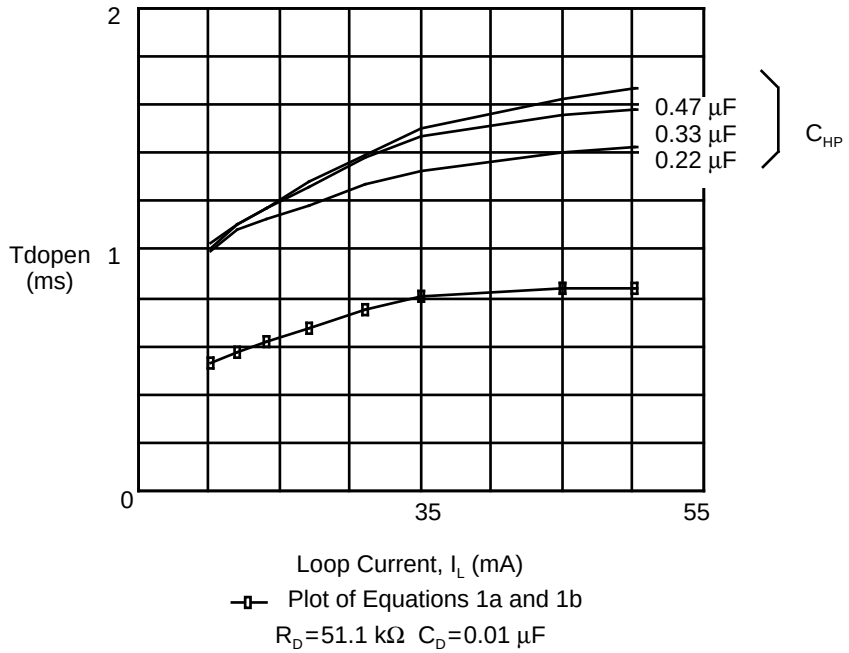

Figure 4f. Tdopen versus I_L for Various C_{HP} (Current Feed Devices)

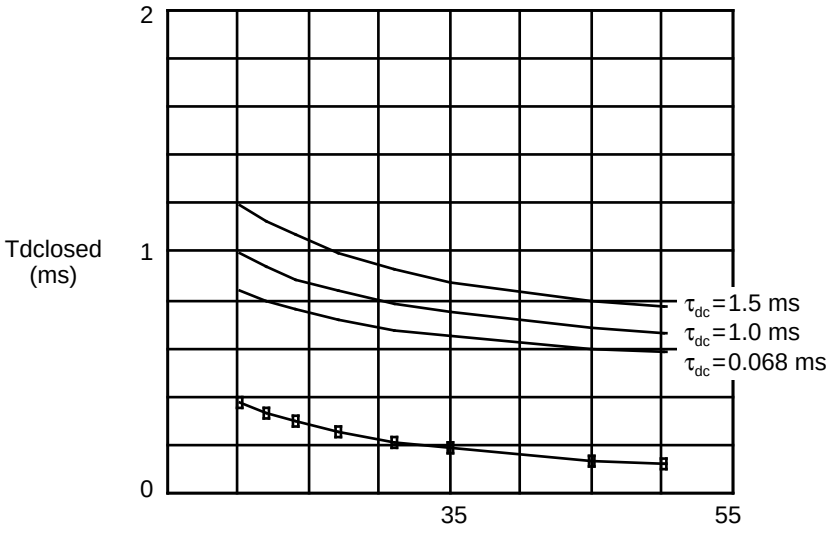

Figure 4g. Tdclosed versus I_L For Various τ_{dc} (Current Feed Devices)

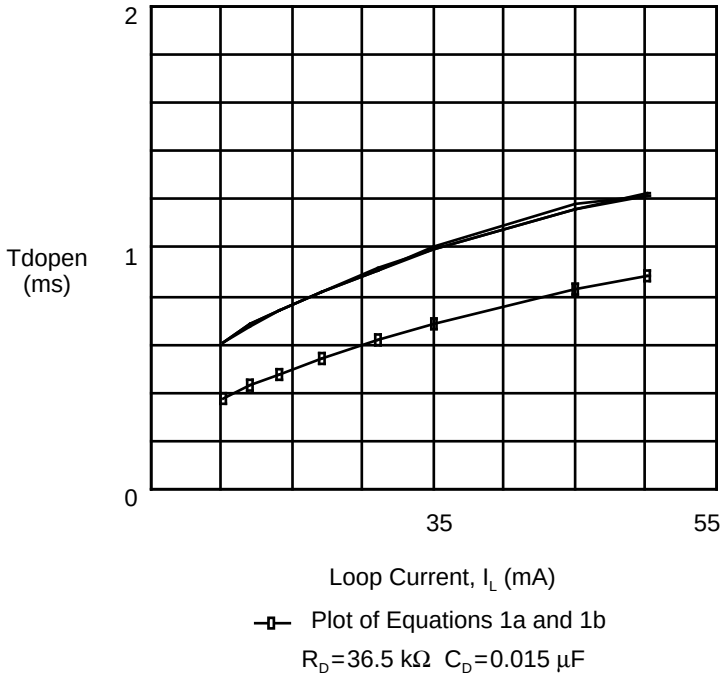

Figure 4h. Tdopen versus I_L (Current Feed Devices)

Component Recommendations

For optimum linecard performance, it is recommended that the following guidelines be considered when selecting values for R_D, C_D, τ_{dc}, and C_{HP}.

Component	Value Range	Comments
R_D	Less than or equal to 51 kΩ	Values greater than 51 kΩ may lead to unacceptable switch hook detection delays.
C_D	0.01 µF	Ensures high frequency noise rejection. (Other values can be used depending on system requirements.)
τ_{dc}*	0.05 to 1.5 ms	Higher values may lead to: 1. Low DC loop stability margins particularly with complex AC impedance synthesis networks. 2. Increased Tdclosed. Lower values may increase the idle channel noise in the anti-saturation region.
C_{HP}	0.22 to 0.47 µF	Higher values lead to increased Tdopen. Lower values lead to an increase of longitudinal voltage generation and possible reduction of DC feed control loop stability margins.

Note:

*To ensure adequate DC control loop stability margins: $C_{HP} \geq \frac{\tau_{dc}}{5000}$.